Two Photo-Mask Fully Self-Aligned Al Bottom-Gate a-Si:H TFTs

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ABSTRACT

A two-photomask fully self-aligned (FSA) pure Al-gate hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) was fabricated. Our FSA a-Si:H TFT had a field-effect mobility and a threshold voltage of 0.58 cm^2/Vs and 14.56 V, respectively, in saturation mode, and an OFF-current and an ON/OFF current ratio of $2.4x10^{-13}$ A and $2.25x10^7$, respectively. This FSA a-Si:H TFTs can enable high-resolution active-matrix liquid-crystal displays (AM-LCDs).

INTRODUCTION

In the past, several researchers have introduced inverted-staggered self-aligned hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) structures to reduce capacitive parasitic component of the TFT gate delay[1,2,3,4,5]. In all structures, the source/drain electrodes were aligned with the gate electrode by back-substrate exposure technique[3]. This photo-lithographic technique simplified the fabrication of the TFTs. However, the major drawback of this technique is that the intrinsic a-Si:H layer needs to be very thin to allow the UV-light to pass through a-Si:H layer for patterning of the source/drain electrodes. The thickness of the gate electrode should also be very thin in order to reduce the step coverage resulting in increased resistive parasitic component of gate delay[1,2,3,4,5]. In this paper, we describe two technologies, pure Al-gate metallization and fully self-aligned (FSA) TFTs that will allow decreasing both capacitive and resistive parasitic components of the gate delay. A new fully self-aligned back-channel etched (BCE) Al-gate a-Si:H TFT was developed during this work to reduce the parasitic capacitance and to take advantage of both a high-performance BCE TFT structure and a low resistivity of Al metallurgy. Our new fully self-aligned BCE Al-gate a-Si:H TFT required only two masks, incorporating anodic aluminum oxidation and back substrate exposure technique.

DEVICE FABRICATION

The fabrication steps of an inverted staggered a-Si:H TFT are shown in *Figure 1*. First, a Al gate electrode was defined on a Corning 1713 glass substrate followed by anodic oxidation (mask #1)[6]. Then the n^+ a-Si:H/a-Si:H/a-SiN_x:H layers were deposited by PECVD technique in one-pumpdown at substrate temperature of 300 °C. A successive deposition of different layers in one pumpdown is essential for stable TFT performance.

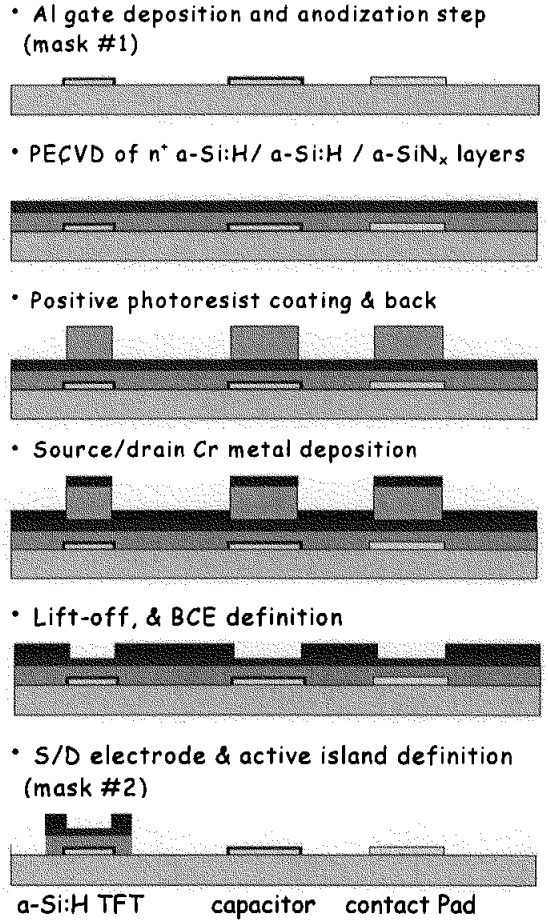


Figure 1. Back-channel-etched FSA a-Si:H TFT process flow. The rest of the AM-LCD process steps are not shown here.

Next, positive photoresist (Microposit 1827) was coated on the top and illuminated by UV-light from the glass substrate side (back-substrate exposure). The a-Si:H and n^+ a-Si:H layers should be very thin to allow exposure of the photoresist, since a-Si:H layer light absorption is film thickness dependent. The UV wavelength that can be used for back exposure ranges from 365 to 405 nm. In this experiment, the transmittance of the UV-light

was about 91 and 100 % for Corning 1713 glass substrate and a-SiN_x:H film, respectively, *Figure 2*. However, the UV-light transmittance was below 15 % for n^+ a-Si:H and a-Si:H layers up to 400 Å thick. There was no transmitted UV-light at all for a-Si:H layers thicker than 1000 Å.

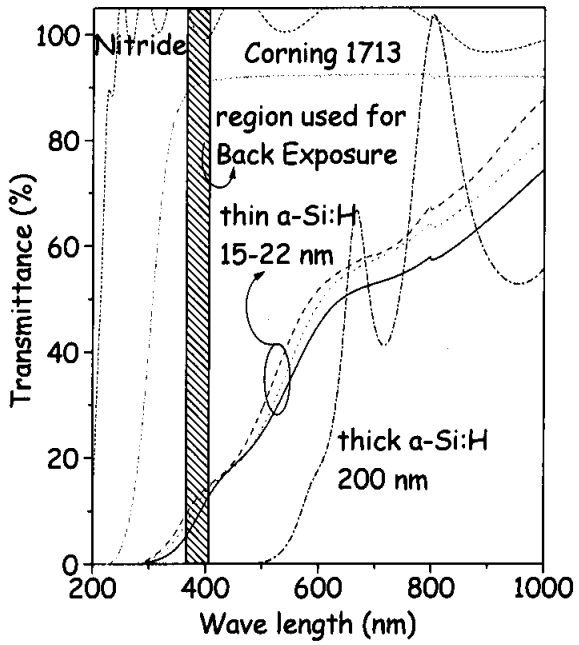


Figure 2. The UV-Visible transmittance spectra for different thin film layers deposited on Corning 1713 glass substrate. The hatched area is the UV-light range used for back exposure by mask aligner.

Because of this important limitation, this fully self-aligned a-Si:H TFT process can only work for a-Si:H layer having thickness less than 100 nm. This can cause some shortcomings related to gate electrode step coverage and requirement to precisely control the back-channel-etch process. However, there are also many other advantages such as smaller number of photomasks, a uniform TFT characteristics, a high manufacturing throughput, and a small parasitic capacitance. To overcome the gate electrode step coverage, the Al gate electrode sidewall profile was tapered during the patterning in a wet etchant solution of a mixture of phosphoric acid, nitric acid, acetic acid, and DI water. After the photoresist development, the photoresist pattern remains just above the gate electrode.

Next, a chromium (Cr) metal layer was deposited at the room temperature by DC magnetron sputtering. After lift-off process, only TFT channel area over gate is opened, with n^+ a-Si:H layer uncovered. The lift-off was done in the hot liquid, 1112A, under the ultrasonic agitation. The channel etch-back of n^+ a-Si:H was carried out using RIE method with O_2 and CCl_2F_2 plasmas. Then, the source and drain electrodes were patterned with photomask (mask #2). The Cr etching was done with the mixture of acetic acid and cerric ammonium nitrate. A RIE etching of n^+ a-Si:H and a-Si:H layers followed the wet etching of the source/drain area to avoid additional photomask for active-island definition. The typical thickness of each layer was 700 Å for Al, 3000 Å for a-SiN_x:H, 220 Å for a-Si:H, 100 Å for n^+ a-Si:H, and 1500 Å for Cr.

EXPERIMENTAL RESULTS AND DISCUSSION

A SEM photograph of a self-aligned BCE a-Si:H TFT with a gate length of 7 μm is shown in the *Figure 3*. The overlap between the gate and the source-drain electrodes was about 1 μm and was found to be uniform over a 4 inch-round substrate.

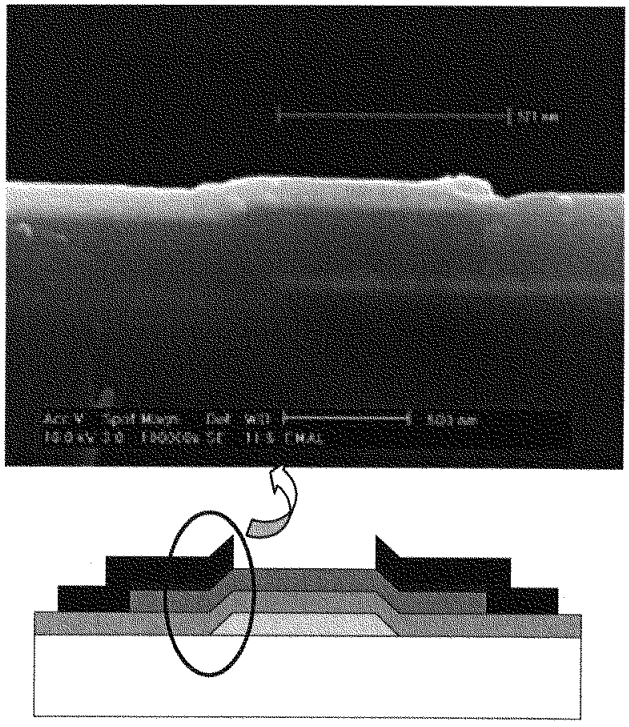


Figure 3. SEM picture of FSA BCE Al-gate a-Si:H TFT. The overlap between gate and source/drain electrodes is 921 nm.

This source/drain - gate overlap is attributed to the light diffraction effect during the back exposure. Changing the exposure and development times can allow controlling the overlap length. This length can range between 0.4 and 1 μm. In conventional a-Si:H TFT used in AM-LCDs, the misalignment during photo-alignment produces a

variation of the source/drain – gate overlap over a display area resulting in an image distortion.

To reduce the effect of the misalignment error, the conventional a-Si:H TFTs are typically designed to have an overlap length of about 3 μm. This large source/drain – gate overlap increases parasitic capacitance and the RC-time delay of the scan bus lines. In addition, the scaling of the TFT size is limited, which leads to the limitation on the scaling down of the pixel size of the AM-LCD.

As seen from the *Figure 4*, the maximum size and the resolution of the AM-LCD, calculated using a sophisticated circuit analysis, are increased substantially for given gate metallurgy when the FSA a-Si:H TFTs are used. In the case of 22 " AMLCD, only FSA a-Si:H TFT with Al gate metallurgy can achieve XGA resolution. In this case, the pixel size is assumed to be 430 μm by 430 μm.

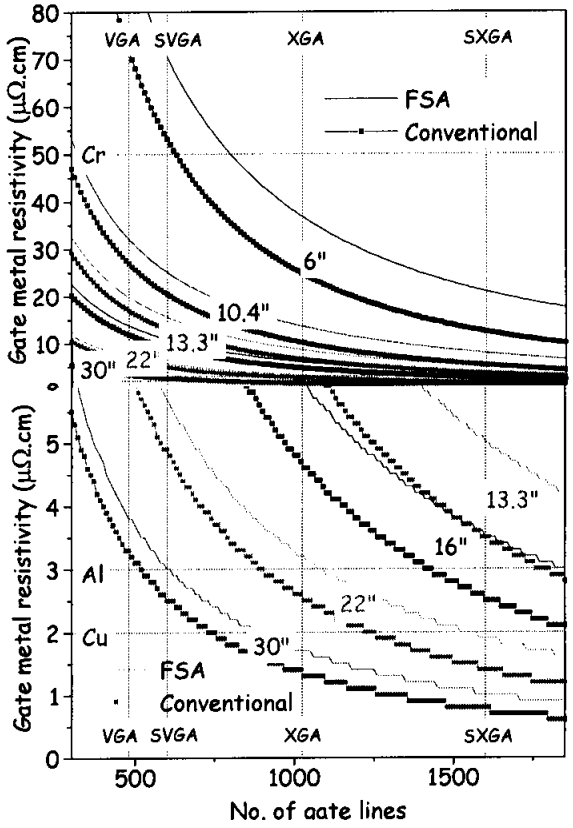
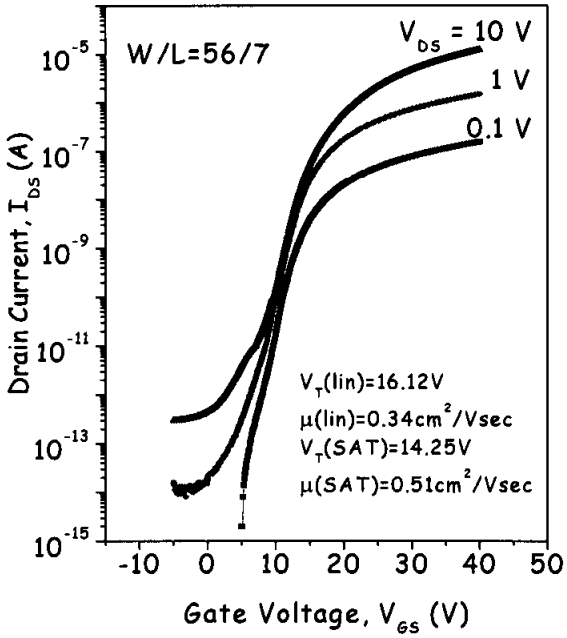
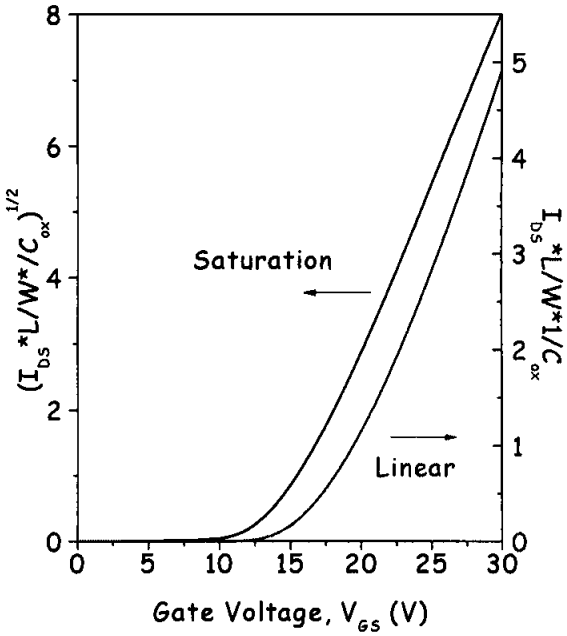


Figure 4. The influence of the gate line delay on display size and resolution for different a-Si:H TFT technologies is shown.

Figure 5 (a) shows the drain-source current (I_{DS})-gate-source voltage (V_{GS}) curves of FSA TFT. The TFT parameters are extracted using a gradual channel approximation in the linear and the saturation regions, *Figure 5 (b)*. This device had a field-effect mobility and a threshold voltage of 0.58 cm^2/Vs and 14.56 V, respectively, in saturation mode, and a OFF-current and a ON/OFF current ratio of $2.4x10^{-13}$ A and $2.25x10^7$, respectively.



(a)



(b)

Figure 5. (a)The I_{DS} versus V_{GS} characteristics of FSA BCE Al-gate a-Si:H TFT, and (b) The characteristics normalized to W/L ratio and gate capacitance, in the linear and saturation regions, respectively.

The rather high threshold voltage of this FSA a-Si:H TFT may result from a very thin a-Si:H layer

having a large density of the deep gap states. It is well known that a-Si:H defect density increases with the increasing film thickness.

A thin a-Si:H layer FSA TFT demonstrated an additional advantage over conventional inverted-staggered a-Si:H TFTs. For different size FSA TFTs, the field-effect mobility and the threshold voltage showed no channel length dependence over channel length between 7 and 620 μm, *Figure 6.* This can to be attributed to a small non-linear access resistance, since the length of the access resistance is very close to the thickness of the intrinsic a-Si:H. Hence, thin a-Si:H layer shortens the length between the conduction channel edges and the source/drain electrodes, effectively reducing the non-linear access resistance.

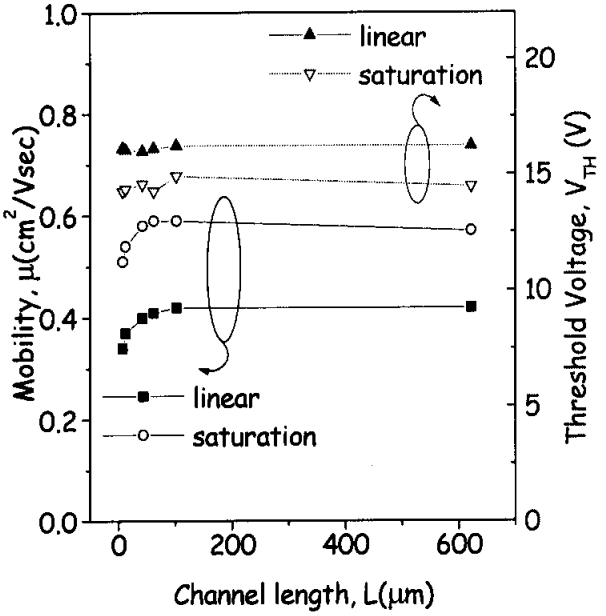


Figure 6. The field-effect mobility and threshold voltage variation with channel length.

The lack of current crowding in our FSA Al-gate a-Si:H TFT I_{DS}-V_{DS} characteristics also support the idea of a small access resistance mentioned above, *Figure 7* (inset). These results demonstrate that the FSA Al-gate a-Si:H BCE TFTs are suitable for application in large-area and high-resolution AM-LCDs.

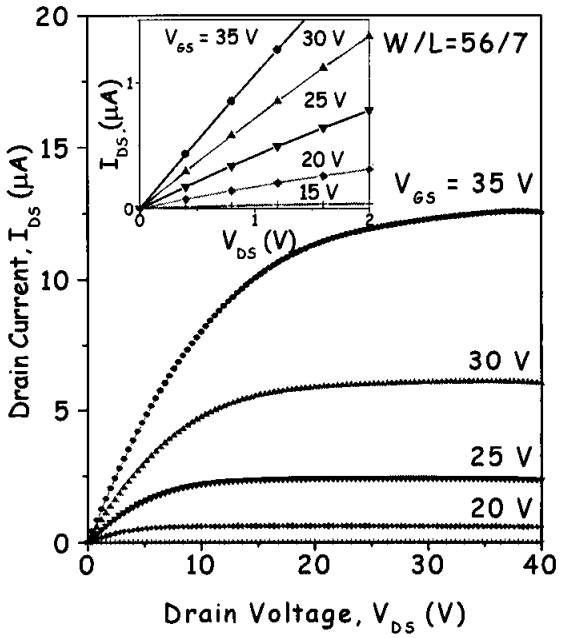


Figure 7. The I_{DS} versus V_{DS} characteristics of FSA BCE Al-gate a-Si:H TFT. An inset shows details of the characteristics near the origin.

CONCLUSOIN

We have fabricated the first FSA Al-gate BCE a-Si:H TFTs for large-area and high-resolution AM-LCDs with only two photo-mask steps using back exposure technique. This FSA a-Si:H TFT technology developed during this study should allow further increase of the AM-LCD size by reducing gate line RC-time delay substantially, which limits the size and resolution of the AM-LCDs. The advantage of this technology was clearly demonstrated during this study.

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